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CERTIFICATE OF FACSIMILE

I hereby certify that this correspondence (along with any paper referred to as being attached or enclosed) is being transmitted via facsimile to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 at (571)-273-8300.

Date: Dec 19 2005

Gregory Turocy

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Applicant: Avanzino, *et al.*

Serial No: 10/755,215

Filing Date: January 12, 2004

Examiner: Stanley J. Pruchnic

Art Unit: 2859

Title: **FABRICATION OF TEMPERATURE SENSING RESISTIVE ELEMENTS ON A HIGH POWER DISSIPATION DEVICE TO MONITOR TEMPERATURE GRADIENTS**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. §1.131

Dear Sir:

We, Steven C. Avanzino and Bharath Rangarajan, declare and say as follows:

(1) We are the inventors of the claims of the above-identified patent application. This Declaration is submitted to establish conception of the invention described and claimed in the above-captioned application in the United States at a date prior to October 30, 2003, which is the date of patent of Chey et al. (U.S. Patent

6,928,380 B2) and to establish diligence from at least just prior to October 30, 2003 until constructive reduction to practice, January 12, 2004.

(2) To establish conception of the invention claimed in the above-identified application prior to October 30, 2003, copies of the relevant portions of an Invention Disclosure describing the invention are enclosed with this Declaration as Exhibit A. Conception and the written description of the invention contained in the Exhibit A were completed prior to October 30, 2003 in this country. Certain information, such as the actual dates and proprietary information, contained on the documents has been removed from the copies.

(3) Exhibit A, an Invention Disclosure, describes with words and drawings the invention captured by the claims. In particular, the Invention Disclosure indicates integrating temperature sensing elements over a fully fabricated integrated circuit device to detect temperature gradients across the circuit device during the operation of the circuit device. The drawings schematically show a plan view of an exemplary circuit component having an array of temperature sensing elements and a cross-sectional view of a circuit component having a temperature sensor layer positioned thereover.

(4) In view of Exhibit A, it can be seen that the invention claimed in the present application was indeed conceived prior to October 30, 2003.

(5) Before October 2003 and after the date of the Invention Disclosure (which is before October 30, 2003), discussions concerning the Invention Disclosure with the drafting attorney took place, as needed, for the purpose of ensuring the drafting attorney fully understood the contents of the Invention Disclosure.

(6) On or about October 1, 2003, a draft version of a patent application for the instant invention was received from the drafting attorney.

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(10) The executed formal papers and the finalized patent application were filed by the drafting attorney on January 12, 2004 with the USPTO.

We, Steven C. Avanzino and Bharath Rangarajan, hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued therein.

_____
Steven C. Avanzino

_____
Date

_____
Bharath Rangarajan

_____
Date

PRIORITY CODE
A ____ B 39
C ____ D ____

Technical Leader: BHANWAR SINGH—CLASSROOM C-1&2

AMD INVENTION DISCLOSURE TLD ID# H0262 Rec'd date ____

California & Asia: x42110, return to MS68; Texas: x55964 return to MS562; Dresden & Europe: x83401 Silke Kretzschmar at MS E21-PP.

This invention applies to: Project: ☐, Product: ☐, Process: ☐, Technology ☐, Other ☐,

IMPORTANT Please identify any potential use: ____

List 2 to 5 key search words related to the invention: ____

Working title of invention: Fabrication of Temperature Sensing Resistive Elements Atop the Interconnect Wiring on a High Power Dissipation Device to Monitor Temperature Gradients

→*INVENTOR/SESSION PARTICIPANT ADDRESS INFORMATION IS ON THE NEXT PAGE (1A)*←

Inventor's signature : ____ **date :** ____
Inventor's printed full name: Steve Avanzino Citizenship: ____
Employee #: ____ Extension: ____ Mail stop: ____ Home telephone:( ) ____
AMD email address: ____ AMD office FAX:( ) ____
Division: ____ Directorate: ____ Dept #: ____ Dept : ____ Manager: ____
Residence address: ____
Post Office address: ____

Co-Inventor's signature : Bharath Rangarajan **date :** ____
Co-Inventor's printed full name: ____ Citizenship: ____
Employee #: ____ Extension: ____ Mail stop: ____ Home telephone:( ) ____
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HARVESTING LAW FIRM/ATTORNEYS: AMIN & TUROCY:
Himanshu Amin, Deborah Corpus and Greg Turocy

Witness 1 initial: ____ Witness 2 initial: ____

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California & Asia: x42110, return to MS68; Texas: x55964 return to MS562; Dresden & Europe: x83401 Silke Kretzschmar at MS B21-PP.

Identify known relevant art (patents, publications, other information): _____

State the problem solved by the invention: Power dissipation and its management is a critical issue in the design of uProcesors and fabrication processes. A means to detect temperature/gradients across a device during operation is useful in this effort.

Brief description and sketch of the invention (*please attach copies of documents like AMD patent notebook pages, reports and drawings that are helpful indescribing / understanding the invention*):

It is proposed that a temperature map of the IC surface can be obtained by providing a dense array of temperature sensing elements integrated onto the surface of the fully processed integrated circuit. These elements may be, for example an array of Kelvin resistor structures, whose individual resistance values will vary as a function of temperature (TCR).

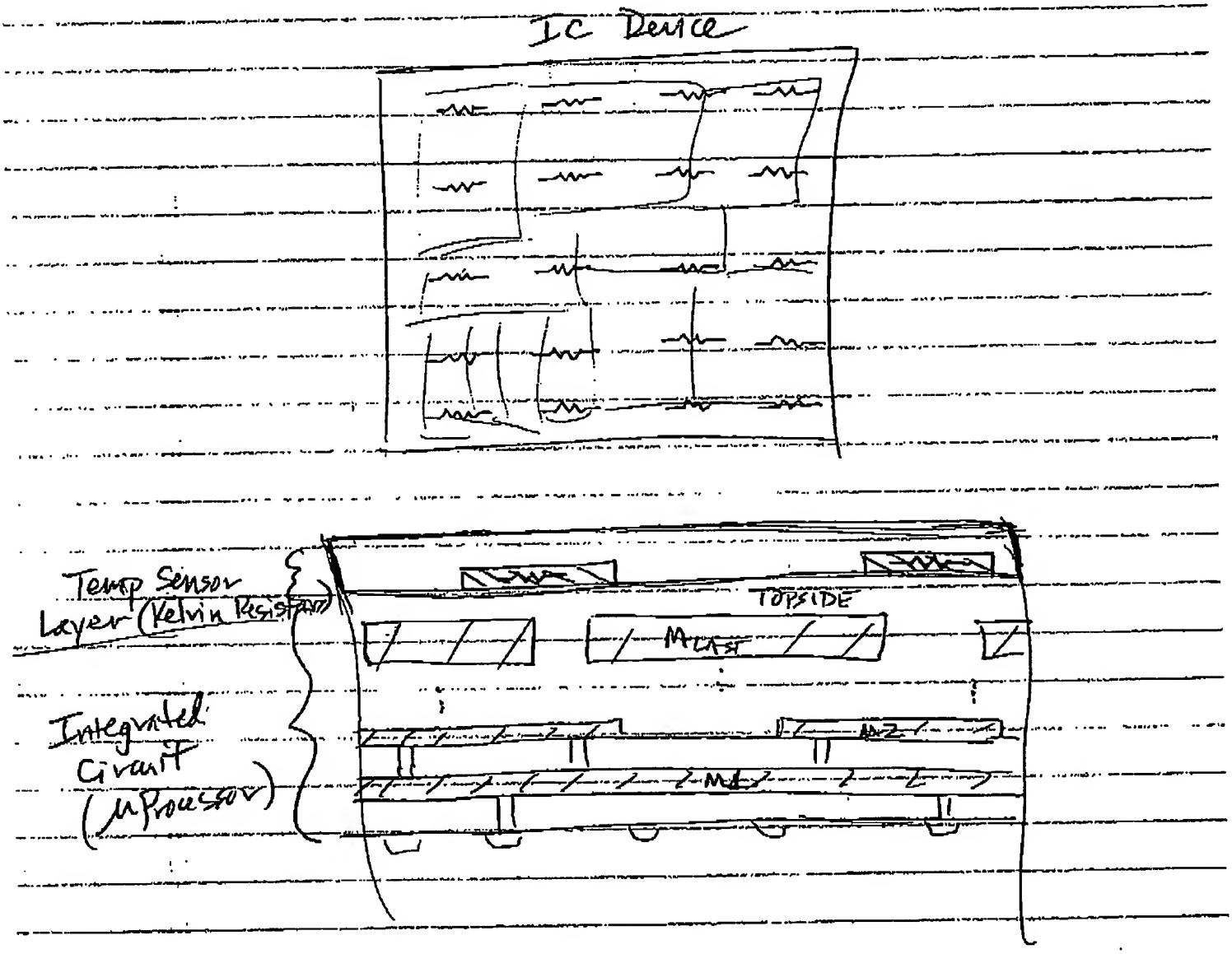
During operation of the circuit, the local regions of the device that generate greatest Joule heating will experience elevated temperature resulting in small temperature gradients. These gradients can be detected + characterized by the Kelvin resistor array.

By fabricating the resistor array on the top of the device, one can maintain the fully-functional IC, yet integrate a micro-fabricated temperature sensing array.

Patent notebook # _____ Page numbers_____ Number of drawings_____

Witness 1 initial: _____ Witness 2 initial: _____

39


IC Device
Temp Sensor Layer (Kelvin Resistor)
Integrated Circuit (uProcessor)
TOPSIDE
M LAST
M2
M1

FRIDAY, MAY 3, 2002
ADVANCED INTEGRATION METROLOGY PATENT HARVEST[illegible]SES[illegible]N
Technical Leader: BHANWAR SINGH—CLASSROOM C-1&2

35

PRIORITY CODE
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AMD INVENTION DISCLOSURE

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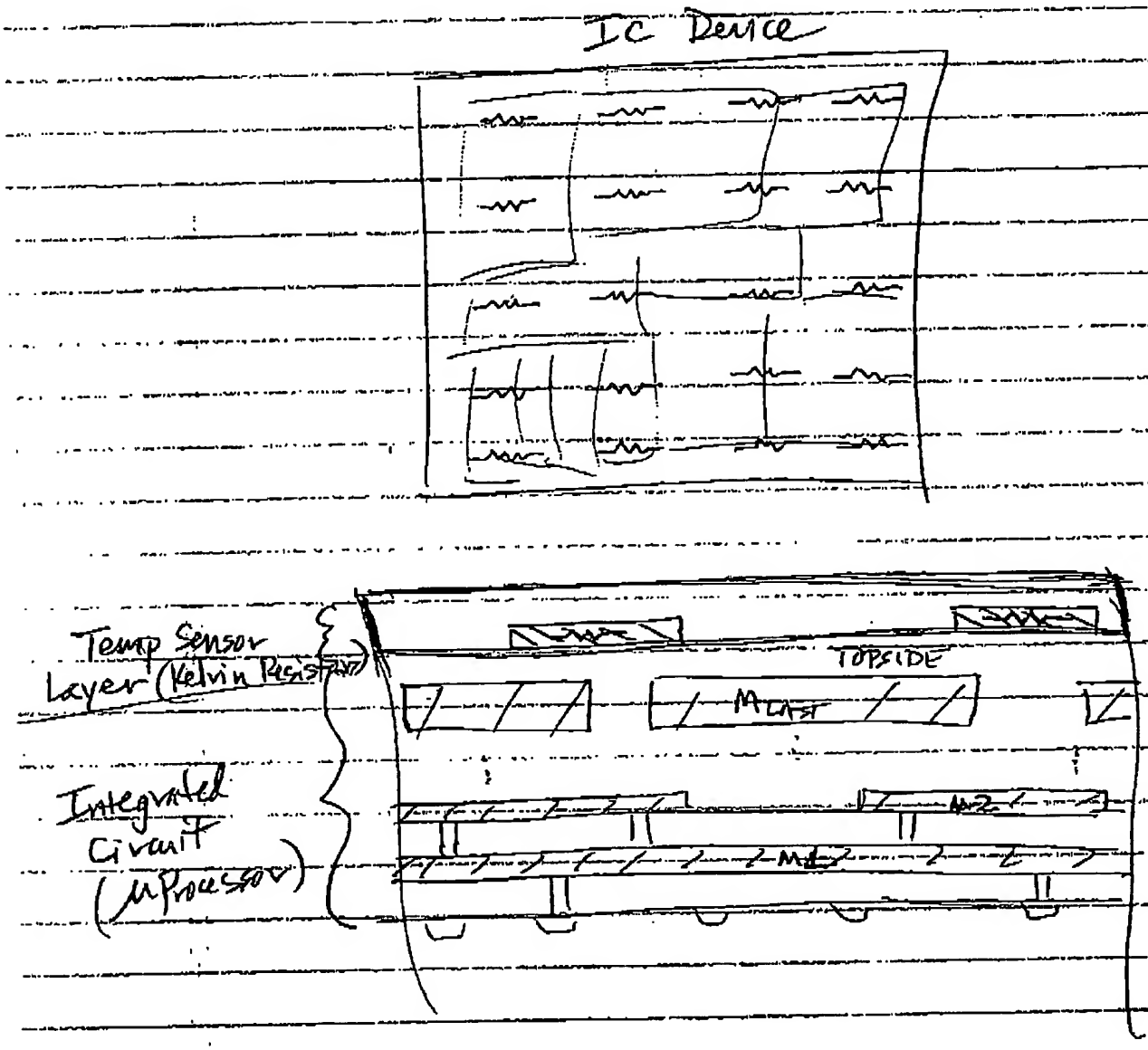
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11/28/05
Date

Bharath Rangarajan

11/28/05
Date

PRIORITY CODE
A ____ B 39
C ____ D ____

Technical Leader: BHANWAR SINGH—CLASSROOM C-1&2

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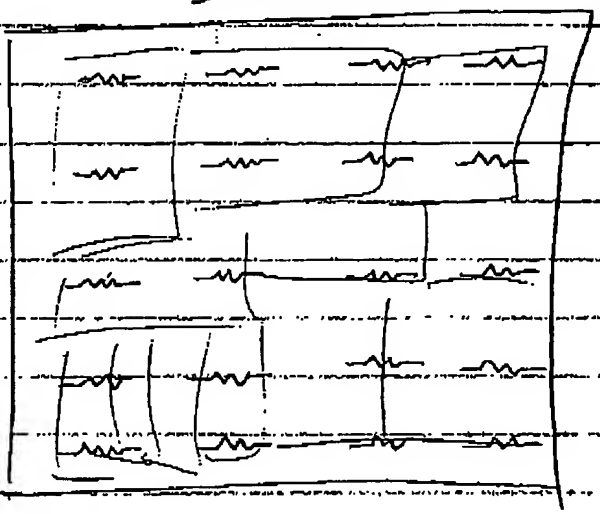
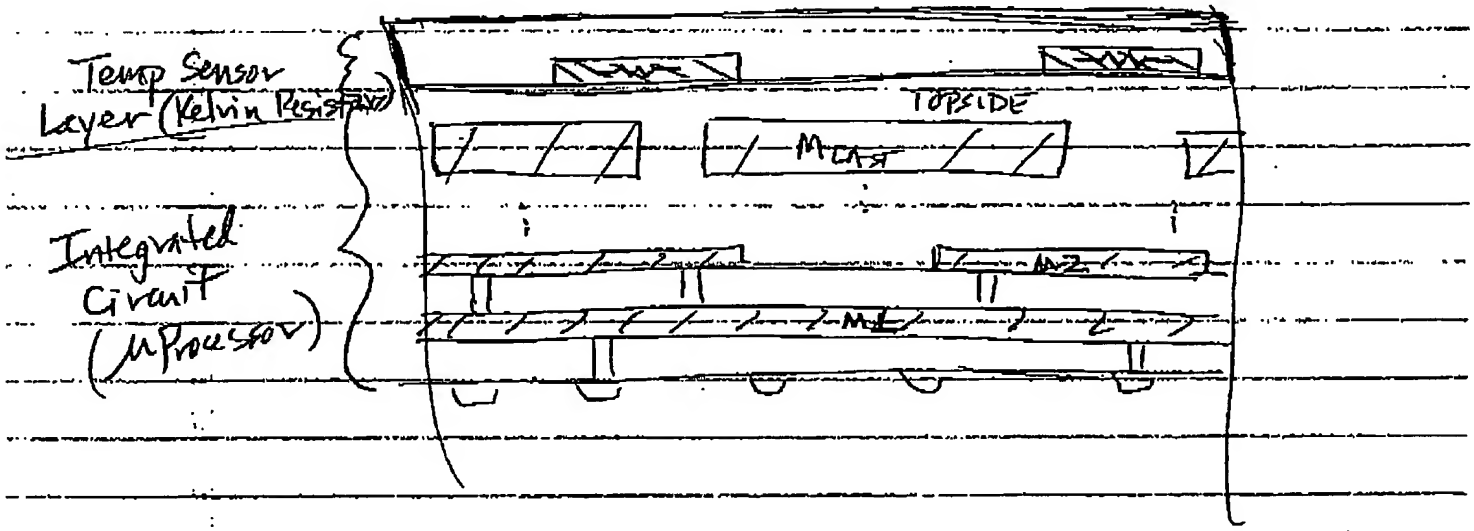
IC Device




Temp Sensor Layer (Kelvin Resistor)
Integrated Circuit (uProcessor)
TOPSIDE
M1
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